

University of Bahrain
College of Information technology
Department of Computer Engineering

Test (2)

Student Name	
I.D. No.	
Section	

Course Title: Digital Logic
Course number: ITCE 202-ITCE 250
Semester: 1
Academic Year: 2012/2013
Duration : 1 hour
Date: 23rd December 2012

*Model
Answer*

Read the following before you start:

1. Write your name, ID and section number
2. Answer all questions.
3. Write your answers on the attached sheets only.

Question	Mark	Mark attained
1	25	
2	25	
3	25	
4	25	
Total	100	

Question [1]: [25 mark]

- a- Give the truth table and the output' equations $\text{Sum} = f(a,b,\text{cin})$ and $\text{Cout} = f(a,b,\text{cin})$ of a Full Adder.

A	B	Cin	Sum	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

T.T

$$\begin{aligned} \text{Sum} &= \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC \\ &= \bar{A}(\bar{B}C + B\bar{C}) + A(\bar{B}\bar{C} + BC) \\ &= \bar{A}(\bar{B} \oplus C) + A(B \oplus \bar{C}) \\ &= A \oplus B \oplus C \end{aligned}$$

$$\text{Cout} = AB + AC_{in} + BC_{in}$$

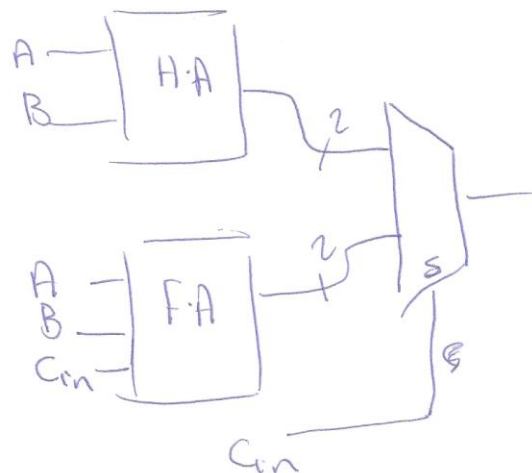
- b- Give the truth table and the output' equations $\text{Sum} = f(a,b)$ and $\text{Cout} = f(a,b)$ of a Half Adder.

A	B	Sum	Cout
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

$$\begin{aligned} \text{Sum} &= \bar{A}B + A\bar{B} \\ &= A \oplus B \end{aligned}$$

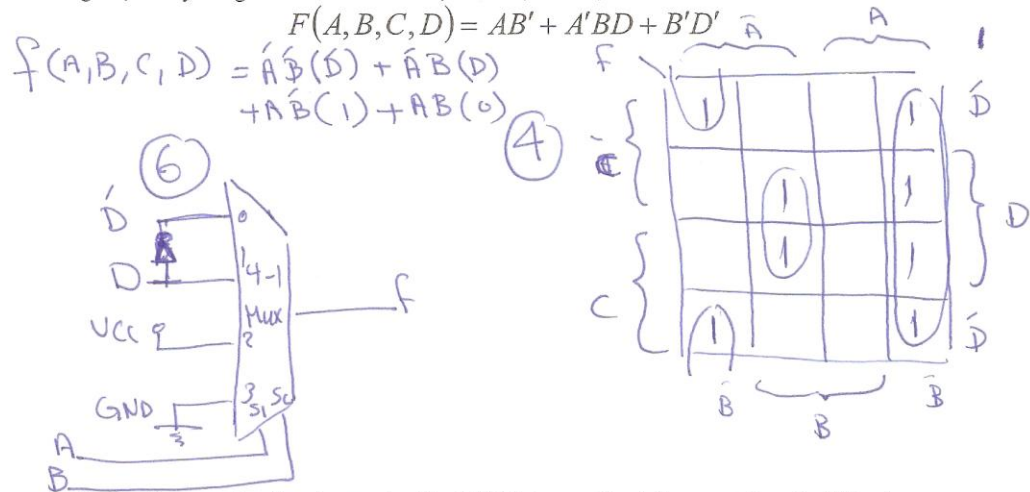
$$\text{Cout} = AB$$

- c- We want to design a circuit that performs an addition of binary bits (a, b and cin) by using a Full or Half Adders. The bit cin is used to select the Full or the Half adders outputs. Give the design and show the different required connections.

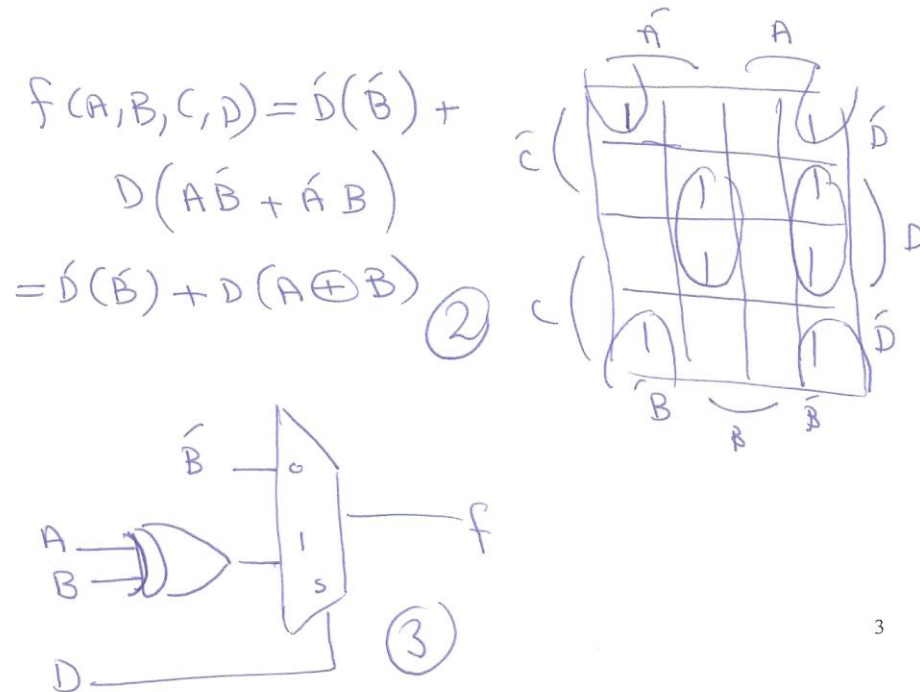


Question [2] : [25 mark]

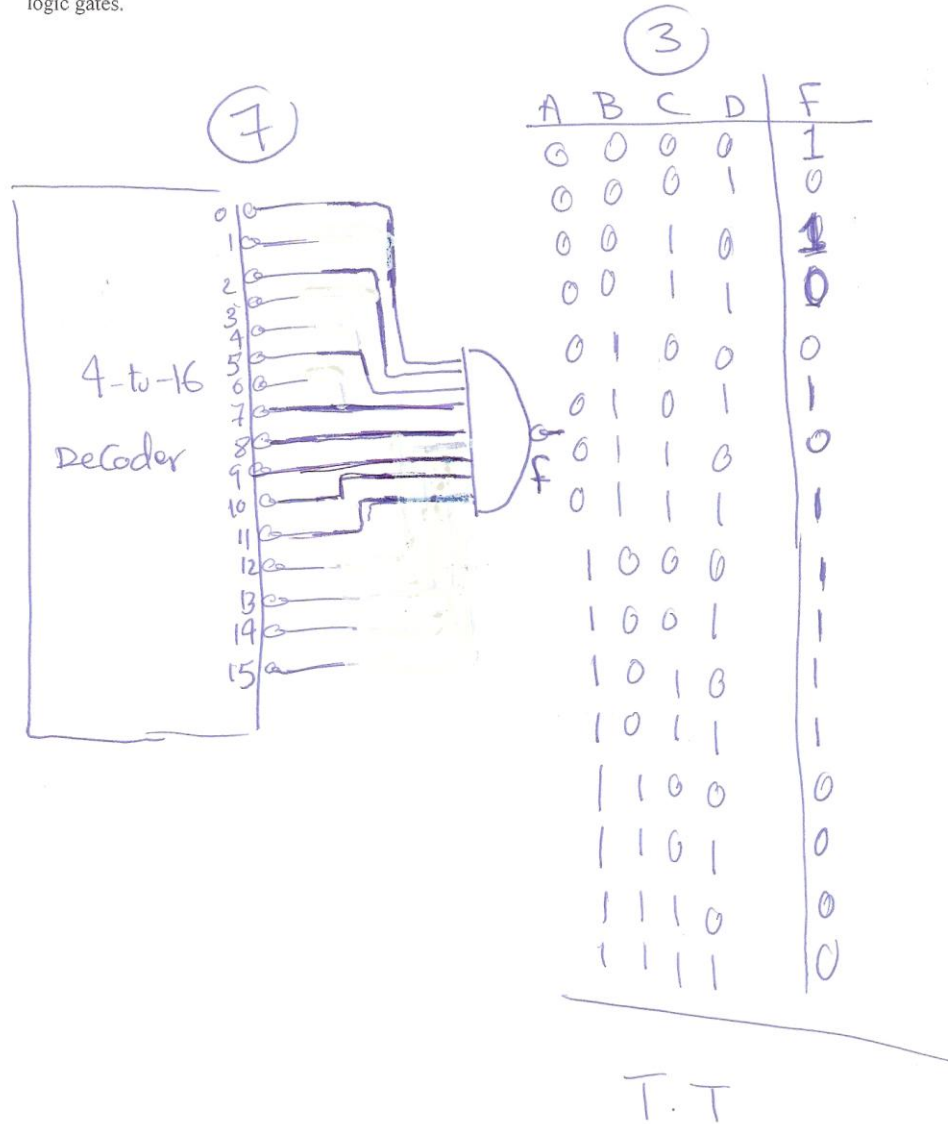
- a. Realize the following function using 4-to-1 Multiplexer with minimum number of additional logic gates, and by using A and B as a selectors, where $S_1=A$ & $S_0=B$:



- b. Realize the same function above using 2-to-1 Multiplexer with minimum number of additional logic gates, and by using D as a selector.



- c. Realize the same function above using 4-16 decoder with inverted outputs and other additional logic gates. (10)



Question [3]: [25 mark]

- a. Write the truth table of a J-K FF, and derive the characteristic (next-state) equation.

J	K	Q
0	0	Q
0	1	0
1	0	1
1	1	\bar{Q}

(5)

J	K	Q	Q ⁺
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

(5)

J	K	Q	Q ⁺
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

(2)

$$Q_{JK}^+ = J\bar{Q} + \bar{K}Q$$

(5)

- i. Complete the given flip flop operation table for the given J-K FF.

CLK	J	K	PreN	ClrN	Q
x	x	x	0	0	not allowed
x	x	x	0	1	1
x	x	x	1	0	0
0	0	0	1	1	Q
0	0	1	1	1	0
0	1	0	1	1	1
0	1	1	1	1	\bar{Q}
0, 1, 2	x	x	1	1	Q

(8)

